REMARKS

Claims 1-4 were examined and reported in the Office Action. Claims 1-4 are rejected. Claim 1 is amended. Claims 1-11 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. §103(a)

A. It is asserted in the Office Action that claims 1 and 4 are rejected under 37 U.S.C. §103(a) as being unpatentable over US Patent No. 6,242, 787 issued to Nakayama et al. ("Nakayama") in view of Applicant's admitted prior art ("AAPA"). Applicant respectfully disagrees.

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 1 contains the limitations of " An HF power device in an HF transistor, comprising: a first semiconductor layer as a first conductive type; a second semiconductor layer formed on the first semiconductor layer; a field area having a trench structure formed in the second semiconductor layer; gate electrode

formed on the second semiconductor layer; a channel layer as a second conductive type laterally diffused from the field area to a width containing both sides of the gate electrode in the second semiconductor layer; a source area as the second conductive type formed within the channel layer between one side of the gate electrode and the field area; a drain area as the second conductive type formed in the second semiconductor layer with a given interval from another side of the gate electrode; a sinker as the first conductive type provided as a column shape of a trench structure for dividing into two source areas by piercing through the source area and the second semiconductor layer, and connected to the first semiconductor layer; an LDD area as the second conductive type formed on the surface of the semiconductor layer between the drain area and the gate electrode; first metal electrode contacted with the source area and electrically connected to the second semiconductor layer through the sinker; and second metal electrode coupled with the drain area.

Applicant's claimed invention provides a power device having an LDMOS device with a sinker formed by using a trench structure. When the sinker is formed through a conventional method, i.e., a diffusion process, there is a problem that a size of the device is increased due to a lateral diffusion during a thermal treatment process to obtain a desired width of the sinker after an ion implantation process. In order to solve the above problem, Applicant's claimed invention uses a trench structure to form the sinker so that the size of the device can be reduced. Also, since the sinker connects the source region to the semiconductor substrate, when a multi-finger device is configured a plurality of source electrodes are not needed.

Nakayama discloses a semiconductor device including a reduced surface field strength type LDMOS transistor that is capable of preventing the breakdown of elements at channel formation portions even when a reverse voltage is applied to its drain. Nakayama, however, does not disclose that a sinker is formed with a trench

structure and is connected to the semiconductor device. Trench structure 123 in Fig. 8 of Nakayama is a field oxide formed to isolate between neighboring devices. The trench structure of Nakayama is quite different from that of Applicant's claimed invention.

It is asserted in the Office Action that AAPA discloses an LDD area as a second conductive type formed on the surface of the semiconductor layer between the drain area and the gate electrode. AAPA, however, does not disclose that a sinker is formed with a trench structure and is connected to the semiconductor device.

Since neither Nakayama, AAPA, or the combination of the two teach, disclose or suggest the limitations contained in Applicant's amended claim 1, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claim 1 is not obvious over Nakayama in view of AAPA since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claim that directly depends from amended claim 1, namely claim 4, would also not be obvious over Nakayama in view of AAPA for the same reason.

Accordingly, withdrawal of the 35 U.S.C. §103(a) rejection for claims 1 and 4 are respectfully requested.

B. It is asserted in the Office Action that claims 2 and 3 are rejected under 35 U.S.C. §103(a) as being unpatentable over Nakayama and AAPA as applied to claim 1, and further in view of U.S. Patent No. 6,326,656 issued to Tihanyi ("Tihanyi"). Applicant respectfully disagrees.

Applicant's claims 2 and 3 depend on amended claim 1. Applicant discussed Nakayama in view of AAPA regarding claim 1 above in section I(A).

Tihanyi discloses a lateral high-voltage transistor that has a semiconductor body made of a lightly doped semiconductor substrate of a first conductivity type and the

epitaxial layer is made of a second conductivity type. Tihanyi also discloses the transistor includes trenches between the source electrode and the drain electrode. The walls of these trenches are highly doped with dopants of the first conductivity type. Tihanyi, however, does not disclose that a sinker is formed with a trench structure and is connected to the semiconductor device.

Since neither Nakayama, AAPA, Tihanyi, or the combination of the three teach, disclose or suggest the limitations contained in Applicant's amended claim 1, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claim 1 is not obvious over Nakayama and AAPA in view of Tihanyi since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claim 1, namely claims 2-3, would also not be obvious over Nakayama and AAPA in further view of Tihanyi for the same reason.

Accordingly, withdrawal of the 35 U.S.C. §103(a) rejection for claims 2 and 3 are respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1-11, patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

PETITION FOR EXTENSION OF TIME

Per 37 C.F.R. 1.136(a) and in connection with the Office Action mailed on WEDNESDAY, MARCH 19, 2003, Applicant respectfully petitions the Commissioner for a two (2) month extension of time, extending the period for response to TUESDAY, AUGUST 19, 2003. The Commissioner is hereby authorized to charge payment to Deposit Account No. 02-2666 in the amount of $205.00 to cover the petition filing fee for a 37 C.F.R. 1.17(a)(2) small entity. A duplicate copy of the fee transmittal is enclosed.

Respectfully submitted,

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Dated: August 18, 2003 By _____

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on August 18, 2003.

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Jean Svoboda